REMARKS

In view of the above amendments and the following remarks, reconsideration of the rejections contained in the Office Action of January 9, 2006 is respectfully requested.

The Examiner rejected claims 1-3 as being anticipated by the Papageorge reference (US 5,438,224). However, the claims have now been amended as indicated above so as to slightly clarify the subject matter recited therein. For the reasons discussed below, it is respectfully submitted that amended claims 1-3 are clearly patentable over the prior art of record.

Independent claim 1 has now been amended to clarify that the module comprises a semiconductor device and a mother multi-layer wiring board on which the semiconductor device is mounted. The semiconductor device includes a *multi-layer wiring board* having a first side and a second side. The multi-layer wiring board includes *a plurality of insulating layers* each having a first side and a second side, and further includes *a plurality of circuit pattern layers* arranged such that one of the circuit pattern layers is located on each of the first side and the second side of each of the insulation layers. The insulation layers and the circuit pattern layers *are alternately laminated.* Each of the insulation layers has a plurality of inner via holes extending between the first side and the second side of each of the insulation layers and electrically connecting the circuit pattern layers so as to define a *three-dimensional wiring pattern.*

The Papageorge reference discloses an integrated circuit package including a substrate 130 with a first IC chip 110 mounted on a first side of the substrate 130 and a second IC chip 120 mounted on a second side of the substrate 130. In the outstanding Office Action, the Examiner asserted that the substrate 130 comprises a multi-layer wiring board with insulation layers 132, 134. However, there does not appear to be any support in the Papageorge reference for the Examiner's interpretation of the substrate 130. Instead, the Papageorge reference explains that the substrate 130 "has a top *surface* 132 and a back *surface* 134 upon which the first IC chip 110 and the second IC chip 120, respectively, are positioned. That is, the first IC chip is placed on the top *surface* 132 and the second IC chip 120 is placed on the bottom *surface* 134 of the interposed substrate 130." (Emphasis added; see column 3, lines 47-53). Thus, reference

numbers 132 and 134 of the Papageorge reference identify opposing surfaces of the substrate 130, rather than multiple insulation layers. The Papageorge reference further explains that the substrate 130 is a flexible circuit substrate with electrical circuitry on its opposite surfaces, with conductive through holes 135 for interconnecting the electrical circuitry and the IC chips 110, 120 mounted on opposite sides of the substrate 130 (see column 3, lines 53-56 and column 4, lines 3-6). There is no description of the substrate 130 as including multiple insulation layers, each having a circuit pattern layer on a first and a second side thereof, and wherein the insulation layers and circuit pattern layers are alternately laminated. Thus, in contrast to the Examiner's interpretation, it is clear that the substrate 130 comprises a *single* insulating layer with a circuit pattern layer on each of the opposite surfaces of the substrate 130.

As noted above, independent claim 1 has been slightly amended so as to clarify the structure of the multi-layer wiring board, and particularly, the plurality of insulation layers and circuit pattern layers alternately laminated to form a three-dimensional wiring pattern. In view of the explanation provided above, it is submitted that the Papageorge reference clearly does not disclose or even suggest a module comprising a semiconductor device and a mother multi-layer wiring board, in which the semiconductor device includes *a multi-layer wiring board* as recited in amended independent claim 1. Thus, it is submitted that the Papageorge reference does not anticipate or even suggest the invention recited in amended independent claim 1. Accordingly, it is respectfully submitted that independent claim 1 and the claims that depend therefrom are clearly patentable over the prior art of record.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance. However, if the Examiner should have any comments or suggestions to help speed the prosecution of this application, the Examiner is requested to contact the Applicant's undersigned representative.

Respectfully submitted,

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